POWER MANAGEMENT INTEGRATED CIRCUITS

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IIT Madras

TYPE OF COURSE : Rerun | Elective | UG/PG
COURSE DURATION : 12 weeks (24 Jan' 22 - 15 Apr' 22)
EXAM DATE : 24 Apr 2022

INTENDED AUDIENCE : Final year undergraduate, graduate, PhD students in Electrical/Electronic Engineering. Faculty, Industry professionals working in the area of analog IC design, VLSI, power management ICs.

PREREQUISITES : Analog Circuits or equivalent or industry experience in analog circuit design

INDUSTRY SUPPORT : Qualcomm, Texas Instruments, Intel, Sankalp Semiconductor, NXP Semiconductors, ST Microelectronics, Samsung, Microchip, ON semiconductor, Infineon, Renesas, Analog Devices

COURSE OUTLINE :

This course is intended to develop understanding of why power management circuits are needed in a VLSI system and what are the different components of a power management system with focus on voltage regulators. By the end of this course, students should be able to understand the concept behind power management circuits and design a linear (LDO) and switching regulator (dc-dc converter) for given specifications using behavioral and circuit level simulators.

ABOUT INSTRUCTOR :

Prof. Qadeer Khan is an Assistant Professor in the Integrated Circuits and System group of the Department of Electrical Engineering, Indian Institute of Technology Madras. He received the Bachelor's degree in Electronics and Communication Engineering from Jamia Millia Islamia University, New Delhi, India, in 1999 and the Ph.D. degree in Electrical and Computer Engineering from Oregon State University, USA in 2012.

COURSE PLAN :

Week 1 : IIntroduction to Power Management;Performance Parameters.

Week 2 : Sub-1-volt Bandgap Reference; Introduction to Linear Regulator, Applications of Linear Regulator;

Week 3 : Miller Compensation, R.H.P. zero due to Miller Compensation, Intuitive Methods of Determining Poles and Zeros after Miller Compensation,

Week 4 : Static Offset Correction, Dynamic Offset Cancellation; Digital LDO, Avoidance of Limit-Cycle Oscillations in a Digital LDO,

Week 5 : Hard Switching Loss, Magnetic Loss, Relative Significance of Losses as a Function of the Load Current;

Week 6 : Compensating a Voltage-Mode-Controlled Buck Converter; Designing Type-I (Integral), Type-II (PI) and Type-III (PID) Compensators;

Week 7 : Designing Type-III Compensator using Gm-C Architecture and Design Example

Week 8 : Designing the Gate-Driver (Gate Buffer and Non-Overlap Clock Generator)

Week 9 : Non-Linear Control Techniques for DC-DC Converters; Hysteretic Control -

Week 10 : Selecting the Process Node for a PMIidelines, Board-Level Layout Guidelines, EMI Considerations

Week 12 : Introduction to Advanced Topics in Power Management (continued)