# MODEL CHECKING

**PROF. SRIVATHSAN.B**
Department of Computer Science and Engineering
Chennai Matematical Institute

**TYPE OF COURSE** : Rerun | Elective | UG
**COURSE DURATION** : 12 weeks (24 Jan' 22 - 15 Apr' 22)
**EXAM DATE** : 23 Apr 2022

**PRE-REQUISITES :** Familiarity with basic algorithms and finite-state machines preferable

**INTENDED AUDIENCE :** This course would be relevant to CSE/EE/ECE/IT students. It would also cater to engineers in the industry who are looking forward to rigorous design and testing methods.

**COURSE OUTLINE :**

Embedded software control many of the safety-critical systems that we deal with in everyday life: for instance, modern cars are equipped with software to automatically change gears; pacemakers come with a software controller to regulate heart beat; aircrafts have flight control software, and so on. Typically, these (software) controllers have to make decisions based on inputs coming from multiple interacting components. As the size and the number of interacting components increase, the design and verification of controllers becomes increasingly complex.

**ABOUT INSTRUCTOR :**

Prof. B. Srivathsan obtained his B. Tech and M. Tech (CSE) from IIT Bombay; and Ph.D from the University of Bordeaux, France. He worked as a post-doctoral researcher at RWTH university - Aachen, Germany. He has been a faculty member at CMI since 2013. His main research interest is in the formal verification of real-time systems.

**COURSE PLAN :**

**Week** 1**:** Modeling systems as Finite-state machines

**Week** 2**:** Using the model-checker NuSMV

**Week** 3**:** Linear-time properties for verification

**Week** 4**:** Regular properties - automata over finite words

**Week** 5**:** Omega-regular properties - automata over infinite words

**Week** 6**:** Model checking omega-regular properties

**Week** 7**:** Linear Temporal Logic (LTL)

**Week** 8**:** Algorithms for LTL

**Week** 9**:** Computation Tree Logic (CTL)

**Week** 10**:** Algorithms for CTL

**Week** 11**:** Binary Decision Diagrams (BDDs)

**Week** 12**:** Models with timing constraints - timed automata Regular properties - automata over finite words