MICROELECTRONICS: DEVICES TO CIRCUITS

PROF.SUDEB DASGUPTA

Department of Electronics & Communication Engineering

IIT Roorkee

INTENDED AUDIENCE : Any Interested Learners

PRE-REQUISITES : First course on linear circuit analysis, A basic course on Semiconductor Devices and
Digital Electronics. A course on Computer Organization will be also helpful (though not strictly required).

INDUSTRIES APPLICABLE TO : Cadence; Synopsys; ST Microelectronics; NXP Semiconductors;Semiconductor Complex Limited; Design House in general

COURSE OUTLINE :

This course is intended for the core courses in Electronics Circuits taught to undergraduates in Electrical and Computer Engineering. The objective of this course is to develop the ability to analyse and design electronic circuits both analog and digital, discrete and integrated. The course starts with the basics of the device most seldom encountered in mixed designs and then go on to do circuit analysis in the later parts.

ABOUT INSTRUCTOR :

Prof. S. Dasgupta,is presently working as an Associate Professor, in Microelectronics and VLSI Group of the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He received his PhD degree in Electronics Engineering from Institute of Technology-Banaras Hindu University (currently IIT-BHU), Varanasi in 2000. During his PhD work, he carried out research in the area of effects of ionizing radiation on MOSFET. Subsequently, he was member of faculty of Department of Electronics Engg.,at Indian School of Mines, Dhanbad (currently IIT-Dhanbad). In 2006, he joined as an Assistant Professor in the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He is currently the Chairman, Faculty Search Committee of the Department. He has authored/co-authored more than 200 research papers in peer reviewed international journals and conferences. His citations are around 2400 (after 2006) and h-index and i-index are 25 and 65 respectively. He is a member of IEEE, EDS, ISTE and associate member of Institute of Nanotechnology, UK. He has been a technical committee member International Conference on Micro-to-Nano, 2006; VDAT-2012, 13, 14, 15, 16, 17 and 18. He worked as the Organising Chair and Program Co-Chair for VDAT-2017 held at IIT Roorkee. He is also heading the Technical Program Group for Emerging Devices at VLSI Design Conference. He has presented tutorial in VDAT-2014 and VLSI Design Conference, Bangalore 2015 amongst many others. He has also been member of technical committees of various international conferences. He has presented large number of invited and keynote talk at various technical forum. He was awarded with Erasmus Mundus Fellowship of European Union in the year 2010 to work in the area of RDF at Politecnico Di Torino, Italy. He is the recipient of prestigious IUSSTF to work in the area of SRAM testing at University of Wisconsin at Madison, USA in the year 2011-12. He was also awarded with DAAD Fellowship to work on Analog Design using Reconfigurable Logic at TU, Dresden, Germany in the year 2013. He is the Principal Coordinator for SMDP-C2SD at IIT Roorkee. His areas of interest are Nanoelectronics, Nanoscale MOSFET modeling and simulation, Design and Development of low power novel devices, FinFET based Memory Design, Emerging Devices in Analog Design and Design and development of reconfigurable logic. He has guided/co-guided 15Ph.D scholars. Currently he is supervising 7 candidates leading to their Ph.D degree. He has been awarded INAE Young Engineer Award. Dr. Dasgupta acted as a reviewer for IEEE Transactions on Electron Devices, IEEE Electron Device Letters, IEEE Transactions on Nanotechnology, Superlattice and Microstructures, International Journal of Electronics, Semiconductor Science and Technology, Nanotechnology, IEEE Transactions on VLSI Systems, Microelectronic Engineering, and Microelectronic Reliability amongst other.

COURSE PLAN :

Week 1:

- Bipolar Junction Transistor; Physical Structure and Modes of operation,
- Operation in Active Mode, circuit symbols and conventions,
- BJT as an Amplifier, small circuit model,
- BJT as a switch and Ebers Moll Model,
- Simple BJT inverter and Second Order Effects.

Week 2:

- MOS Transistor Basic,
- MOS Parasitic & SPICE Model;
- CMOS Inverter Basics-I

Week 3:

- CMOS Inverter Basics(contd)
- Power Analysis
- SPICE Simulation-I

Week 4:

- Biasing of MOS Amplifier and its behavior as an analog switch,
- CMOS CS/CG/SF Amplifier Configuration,
- Internal cap models and high frequency modelling,
- JFET, structure and operation.

Week 5:

- Multistage and Differential Amplifier,
- Small Signal Operation and Differential Amplifier,
- MOS Differential Amplier,
- BiCMOS Amplifier with Active Load,
- Multistage Amplifier with SPICE Simulation

Week 6:

- s-domain analysis, transfer function, poles and zeros,
- High Frequency Response of CS and CE Amplifier,
- Frequency Response of CC and SF Configuration,
- Frequency Response of the Differential Amplifier,
- Cascode Connection and its Operation

Week 7:

- General Feedback structure and properties of negative feedback,
- Basic Feedback Topologies,
- Design of Feedback Amplifier for all configuration,
- Stability and Amplifier poles,
- Bode Plots and Frequency Compensation

Week 8:

- Ideal Operational Amplifier and its terminals,
- Inverting and Non- Inverting Configuration,
- As an integrator and Differentiator,
- Introduction to Analog Computer,
- Large Signal Operation of Op-Amp and Second order offsets.

Week 9:

- Butterworth and Chebyshev Filters,
- First and Second Order Filter Functions,
- Switched Capacitor based filters,
- Single-Amplifier Biquadratic Filters,
- Second Order LCR Resonator.

Week 10: Combinational Logic Design

Week 11: Sequential Logic Design

Week 12: Clock Strategies for Sequential Design, Concept of Memory & its Designing-I